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EXAMINER	
NATALINI, JEFF WILLIAM	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/810,645	KER ET AL.	
	Examiner	Art Unit	
	Jeff Natalini	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claim 12 is objected to because of the following informalities:

- A first and second pulse generator is disclosed in this claim, but two pulse generators are not disclosed in any of the figures. Amendments to fix this problem were discussed and approved in a telephone conversation with Clark Jablon on November 22, 2005.

Appropriate correction as discussed is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 10, 12-15, 17-23, 28-29, 31, 32, and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by (Chen et al. "Investigation of the Gate-Driven Effect and Substrate-Triggered Effect on ESD Robustness of CMOS Devices" herein to be referred to as Chen).

In regard to claims 1, 5, 12, 15, 18, 21, and 31, Chen discloses a system for measuring electrostatic discharge (ESD) characteristics of a semiconductor/multi-terminal device (abstract), comprising: at least one pulse generator generating ESD-scale pulses (fig 5a, 8a, 13, or 14)); a first point of the semiconductor device (TLPG-seen as an input into the drain in figs (5a, 8a, 13, or 14)) receiving a first ESD-scale

pulse from the at least one pulse generator, a second point of the semiconductor device receiving the first ESD-scale pulse from the at least one pulse generator (pg 191, fig 4 shows different points of the drain being connected) at least a third point of the semiconductor device receiving a second ESD-scale pulse from a second pulse generator (pg 197 figs 13 and 14 show a biasing source generating a pulse into the gate); and a data collector to collect data on the ESD characteristics of the semiconductor device (abstract states that data is collected and measured and figures on pg 193-195 show that the device was hooked up to display and analyze data); detecting if a leakage current flows in the semiconductor device (pg 194 column 1 continued to col 2; measured leakage currents are shown in fig 8b)).

In regard to claims 2, 17, 22, and 32, Chen discloses wherein the semiconductor device is a MOS transistor (fig 4).

In regard to claims 3, 4, 13, 14, 19, 20, and 35, Chen discloses wherein a transmission line pulse generator is able to generate ESD pulses (abstract; also different pulses are generated in fig 5a pg 192 or 21a pg 202, which allows two different pulses to be TLP driven).

In regard to claim 6 and 23, wherein the MOS transistor includes a source and drain to receive the first ESD pulse (fig 11 pg 196, the ESD pulse is applied to the drain in different positions as seen in fig 4, the source also receives the signal as they are tied together and is seen in the side graphs) and a gate to receive the second ESD pulse (this is seen in figs 12-14 pg 197).

In regard to claims 10 and 29, Chen discloses a detector to detect a leakage current in the device (pg 194 column 1 continued to col 2; measured leakage currents are shown in fig 8b).

In regard to claim 28, Chen discloses a data collector to collect data regarding the ESD characteristics of the semiconductor device (abstract states that data is collected and measured and figures on pg 193-195 show that the device was hooked up to display and analyze data).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9, 26, 27, 31, 32, 33, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen.

In regard to claim 31, Chen discloses Chen discloses a system for measuring electrostatic discharge (ESD) characteristics of a semiconductor/multi-terminal device (abstract), comprising: at least one pulse generator generating ESD-scale pulses (fig 5a, 8a, 13, or 14)); a first point of the semiconductor device (TLPG-seen as an input into the drain in figs (5a, 8a, 13, or 14)) receiving a first ESD-scale pulse from the at least one pulse generator, a second point of the semiconductor device receiving the first ESD-scale pulse from the at least one pulse generator (pg 191, fig 4 shows different

points/terminals of the drain being connected); and a data collector to collect data on the ESD characteristics of the semiconductor device (abstract states that data is collected and measured and figures on pg 193-195 show that the device was hooked up to display and analyze data); detecting if a leakage current flows in the semiconductor device (pg 194 column 1 continued to col 2; measured leakage currents are shown in fig 8b)).

Chen lacks specifically disclosing where a second ESD-scale pulse of the at least two ESD scale pulses to at least the second terminal and a third terminal of the multi-terminal device.

Chen discloses on pg 199 in the paragraph under the heading "Substrate-triggered effect" that the ESD during testing can be increased from 3.5kV to greater than 8kV, and there are different steps in the incremental process (2.8kV to 4.4kV). So by implementing this testing logic on figure 4 the three terminals/points in question (actually four terminals/points are shown in fig 4, but only three are required) would receive a first pulse of say 3.5kV and then all three would receive a second pulse higher than 3.5kV.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chen to incorporate increasing the ESD level of the pulse generator disclosed in fig 4 and provide an increasing pulse to multiple terminals as described on pg 199 under "Substrate-triggered effect" in order to measure the substrate triggered effect (lines 9-11 of the "Substrate-triggered effect" paragraph on pg 199).

In regard to claims 9, 26, and 27, Chen teaches all that is disclosed above to reject claims 6 and 22.

Chen lacks specifically disclosing where in both a FOD and BJT the emitter and collector receive the first ESD pulse, and a base receives the second ESD pulse.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to use engineering intuition knowing that MOSFETS and BJTs/FOTs are similar devices even though are separated by analog and digital realms, the source and drain/similar of a MOS are similar to collector/emitter of FOT/BJT and gate of MOS is similar to the base of FOT/BJT and test the structure accordingly even though it is digital in order to determine proper electrostatic properties of semiconductor devices.

In regard to claim 32, Chen discloses wherein the semiconductor device is a MOS transistor (fig 4).

In regard to claim 33, Chen lacks specifically where the second pulse is supplied to the third terminal before the first pulse is applied to the second and third.

MPEP 21144.04 *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) says that selection of any order of performing process steps is prima facie obvious in the absence of new and unexpected results.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chen to apply the second pulse before the first pulse in order to perform variations of tests so to be able to provide the best analysis on electrostatic properties on semiconductor devices.

In regard to claim 35, Chen discloses wherein a transmission line pulse generator is able to generate ESD pulses (abstract; also different pulses are generated in fig 5a pg 192 or 21a pg 202, which allows two different pulses to be TLP driven).

6. Claims 7, 8, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Ker et al. (US 5576557).

Chen lacks wherein an SCR and LVTSCR includes an anode and a cathode to receive the first ESD pulses, and a substrate to receive a second ESD pulse.

Ker et al. teaches SCR and LVTSCR includes an anode and a cathode to receive an ESD pulse, and a substrate to receive a second ESD pulse.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chen to include testing a SCR and LVTSCR with an anode and cathode to receive an ESD pulse, and a substrate to receive a second ESD pulse as disclosed by Ker et al. in order to be able to provide proper protection to CMOS ICs (col 1 line 11-15).

7. Claims 11, 16, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Consiglio (US 5519327).

Chen lacks wherein there is a switching device coupled to the pulse generator(s) and the detector to switch a connection between the pulse generator(s) and the detector.

Consiglio teaches having a switch coupled between a pulse generator and the detector to detect the leakage current so to switch the connection between the pulse generator and the detector (fig 3, chart; abstract).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chen to include a switch coupled between a pulse generator and the detector to detect the leakage current as taught by Consiglio in order to determine the leakage current after each pulse is applied to the DUT (abstract).

8. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Barth et al. ("TLP Calibration, Correlation, Standards, and New Techniques" herein to be referred to as Barth).

Chen lacks specifically stating wherein a step of detecting whether leakage current flows in the multi-terminal device before providing the first and second ESD-scale pulse.

Barth et al. teaches that the concept of measuring leakage current in TLP test systems is for the user to know how the leakage current evolved as the pulse test current amplitude was increased.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chen to detect whether a leakage current flows before providing the pulses to the device in order to know how the leakage current evolved as the test pulses were increased as taught by Barth et al.

Response to Arguments

9. Applicant's arguments filed 8/19/05 have been fully considered but they are not persuasive. Discussed during the telephone conference November 22 was the differences between an ESD scale pulse and a regular .1 or 1.1 V bias disclosed in figure 13 pg 197 of Chen and discussed on pg 12 line 24-28 of the remarks. Examiner appreciates the further discussion of the difference between the two signals and how the prior art differs. Though upon further analysis of the prior art, claim language, and specification it was decided to uphold the previous rejection. The independent claims (1, 12, 18) all disclose (or in a similar form) "a third point of the semiconductor device receiving a second ESD-scale pulse from the at least one pulse generator". An examiner must interpret the claim language with the broadest reasonable interpretation, unless there is a special definition in the specification. At best the specification pg 1 paragraph 3, describes an "ESD event is an electrical discharge of a current (positive or negative) for a short duration during which a large amount of current is provided to the IC, and this may damage the IC". Short duration and large amount of current is not specific to a certain time period or a particular amount of amps. Also not disclosed in the specification is that the ESD scale pulse is at a certain voltage. Therefore given the broadest possible interpretation the bias source at .1V or 1.1V could broadly be considered an ESD scale pulse, as a device that is rated to withstand only 1 mV will have a electrical discharge of current for a short duration at which a large amount of

current (large for the device) is provided and may cause damage when a .1 or 1.1 V signal is applied.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection (for claims 31-35) presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diane Lee can be reached on 571-272-2399. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeff Natalini

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PRIMARY EXAMINER